



# PCA9531

8-bit I<sup>2</sup>C-bus LED dimmer

Rev. 05 — 12 September 2007

Product data sheet

## 1. General description

The PCA9531 is an 8-bit I<sup>2</sup>C-bus and SMBus I/O expander optimized for dimming LEDs in 256 discrete steps for Red/Green/Blue (RGB) color mixing and back light applications.

The PCA9531 contains an internal oscillator with two user programmable blink rates and duty cycles coupled to the output PWM. The LED brightness is controlled by setting the blink rate high enough (> 100 Hz) that the blinking cannot be seen and then using the duty cycle to vary the amount of time the LED is on and thus the average current through the LED.

The initial setup sequence programs the two blink rates/duty cycles for each individual PWM. From then on, only one command from the bus master is required to turn individual LEDs ON, OFF, BLINK RATE 1 or BLINK RATE 2. Based on the programmed frequency and duty cycle, BLINK RATE 1 and BLINK RATE 2 will cause the LEDs to appear at a different brightness or blink at periods up to 1.69 second. The open-drain outputs directly drive the LEDs with maximum output sink current of 25 mA per bit and 100 mA per package.

To blink LEDs at periods greater than 1.69 second the bus master (MCU, MPU, DSP, chip set, etc.) must send repeated commands to turn the LED on and off as is currently done when using normal I/O expanders like the NXP Semiconductors PCF8574 or PCA9554. Any bits not used for controlling the LEDs can be used for General Purpose parallel Input/Output (GPIO) expansion, which provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push-buttons, alarm monitoring, fans, etc.

The active LOW hardware reset pin ( $\overline{\text{RESET}}$ ) and Power-On Reset (POR) initializes the registers to their default state causing the bits to be set HIGH (LED off).

Three hardware address pins on the PCA9531 allow eight devices to operate on the same bus.

## 2. Features

- Eight LED drivers (on, off, flashing at a programmable rate)
- Two selectable, fully programmable blink rates (frequency and duty cycle) between 0.59 Hz and 152 Hz (1.69 second and 6.58 milliseconds)
- 256 brightness steps
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I<sup>2</sup>C-bus interface logic compatible with SMBus
- Internal power-on reset

- Noise filter on SCL/SDA inputs
- Active LOW reset input
- Eight open-drain outputs directly drive LEDs to 25 mA
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO16, TSSOP16, HVQFN16 (SOT629-1 and SOT758-1 versions)

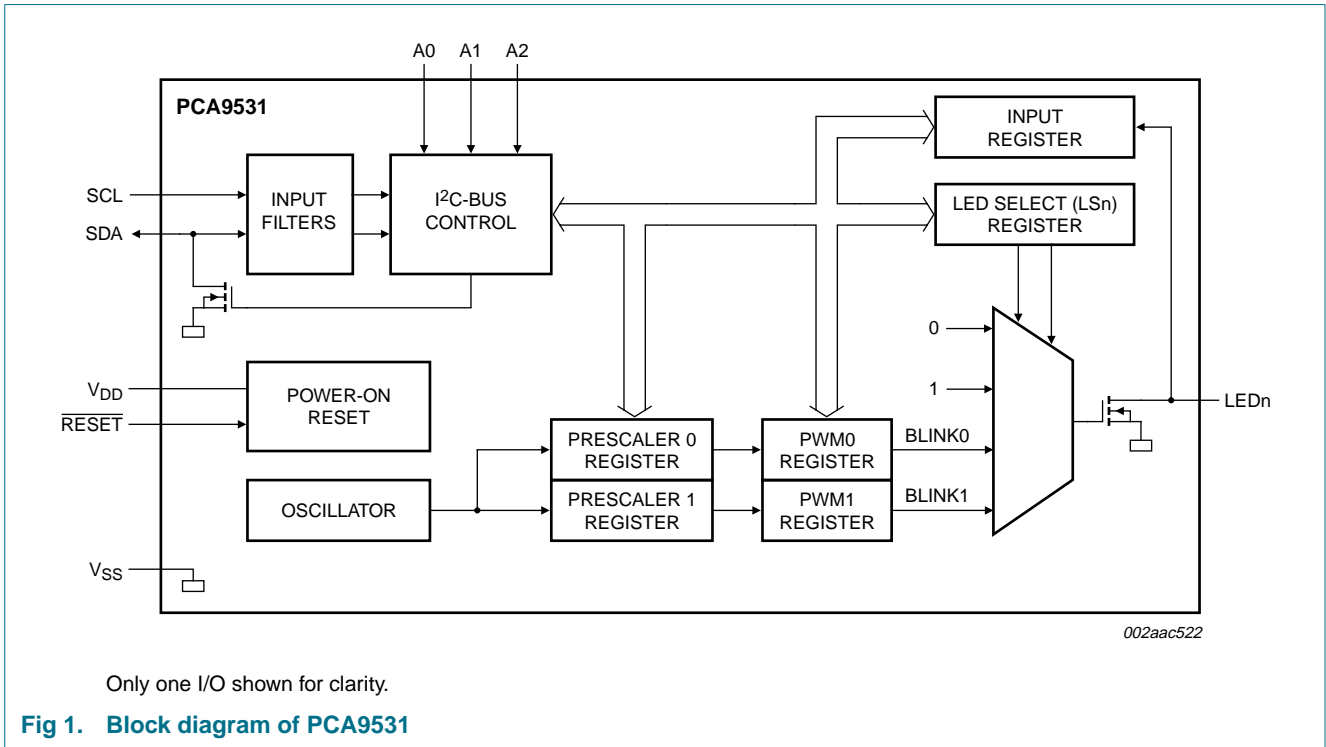
### 3. Ordering information

**Table 1. Ordering information**

*T<sub>amb</sub> = -40 °C to +85 °C.*

| Type number | Topside mark | Package |  |          |
|-------------|--------------|---------|--|----------|
|             |              | Name    | Description  | Version  |
| PCA9531D    | PCA9531D     | SO16    | plastic small outline package; 16 leads; body width 3.9 mm   | SOT109-1 |
| PCA9531PW   | PCA9531      | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm                             | SOT403-1 |
| PCA9531BS   | 9531         | HVQFN16 | plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm | SOT629-1 |
| PCA9531BS3  | 531          | HVQFN16 | plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm | SOT758-1 |

4. Block diagram



## 5. Pinning information

### 5.1 Pinning

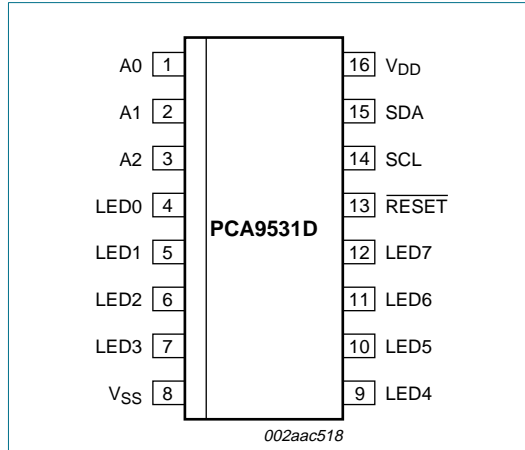


Fig 2. Pin configuration for SO16

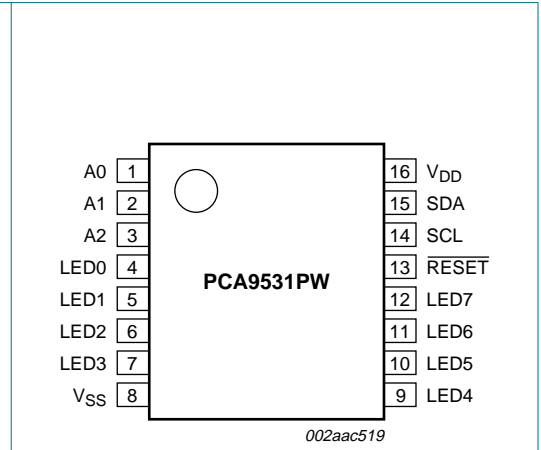


Fig 3. Pin configuration for TSSOP16

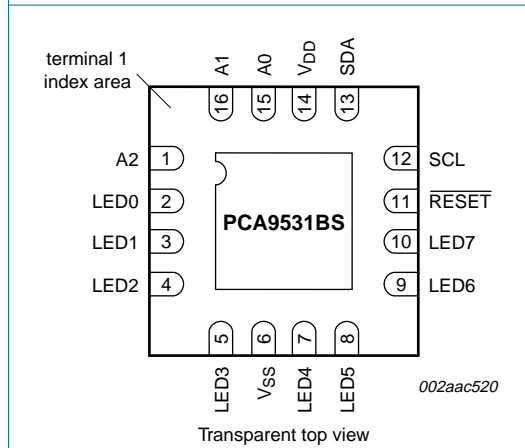


Fig 4. Pin configuration for HVQFN16 (SOT629-1)

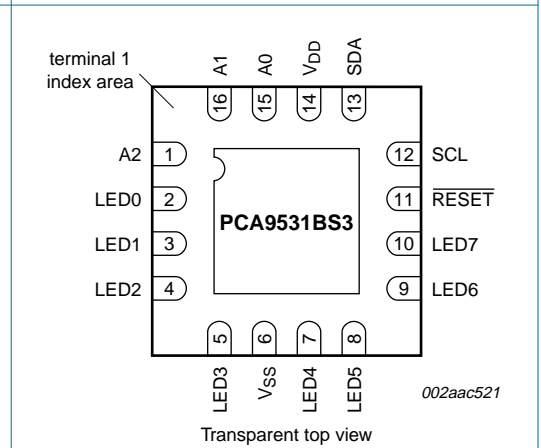


Fig 5. Pin configuration for HVQFN16 (SOT758-1)

### 5.2 Pin description

Table 2. Pin description

| Symbol | Pin           |         | Description     |
|--------|---------------|---------|-----------------|
|        | SO16, TSSOP16 | HVQFN16 |                 |
| A0     | 1             | 15      | address input 0 |
| A1     | 2             | 16      | address input 1 |
| A2     | 3             | 1       | address input 2 |
| LED0   | 4             | 2       | LED driver 0    |
| LED1   | 5             | 3       | LED driver 1    |
| LED2   | 6             | 4       | LED driver 2    |

**Table 2. Pin description ...continued**

| Symbol          | Pin              |                  | Description              |
|-----------------|------------------|------------------|--------------------------|
|                 | SO16,<br>TSSOP16 | HVQFN16          |                          |
| LED3            | 7                | 5                | LED driver 3             |
| V <sub>SS</sub> | 8                | 6 <sup>[1]</sup> | supply ground            |
| LED4            | 9                | 7                | LED driver 4             |
| LED5            | 10               | 8                | LED driver 5             |
| LED6            | 11               | 9                | LED driver 6             |
| LED7            | 12               | 10               | LED driver 7             |
| RESET           | 13               | 11               | reset input (active LOW) |
| SCL             | 14               | 12               | serial clock line        |
| SDA             | 15               | 13               | serial data line         |
| V <sub>DD</sub> | 16               | 14               | supply voltage           |

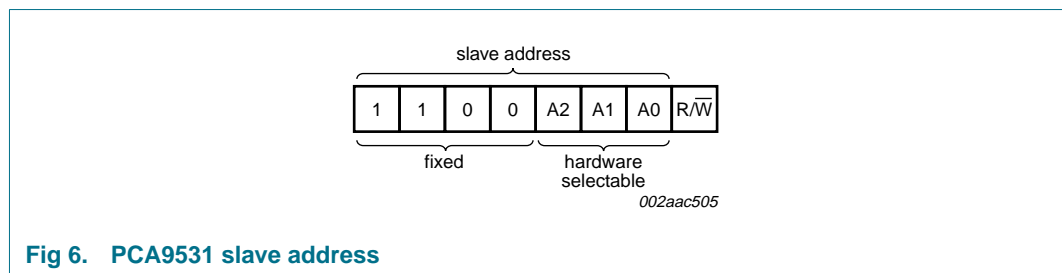
[1] HVQFN package die supply ground is connected to both V<sub>SS</sub> pin and exposed center pad. V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

## 6. Functional description

Refer to [Figure 1 “Block diagram of PCA9531”](#).

### 6.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9531 is shown in [Figure 6](#). To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

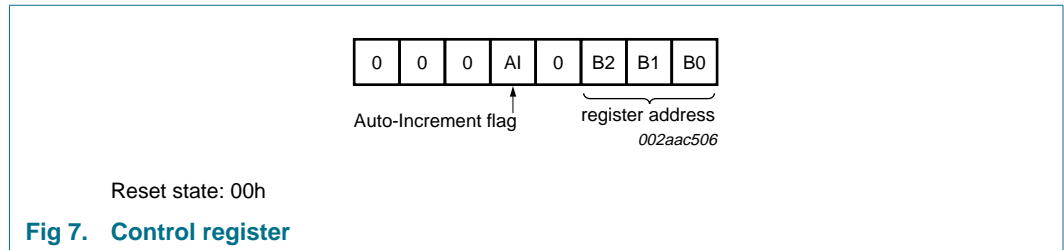


**Fig 6. PCA9531 slave address**

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

## 6.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9531, which will be stored in the Control register.



The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the Auto-Increment flag is set, the three low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '000' after the last register is accessed.

When Auto-Increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from the Input register (B2 B1 B0 ≠ 0 0 0).

Only the 3 least significant bits are affected by the AI flag. Unused bits must be programmed with zeroes.

### 6.2.1 Control register definition

Table 3. Register summary

| B2 | B1 | B0 | Symbol | Access     | Description           |
|----|----|----|--------|------------|-----------------------|
| 0  | 0  | 0  | INPUT  | read only  | input register        |
| 0  | 0  | 1  | PSC0   | read/write | frequency prescaler 0 |
| 0  | 1  | 0  | PWM0   | read/write | PWM register 0        |
| 0  | 1  | 1  | PSC1   | read/write | frequency prescaler 1 |
| 1  | 0  | 0  | PWM1   | read/write | PWM register 1        |
| 1  | 0  | 1  | LS0    | read/write | LED0 to LED3 selector |
| 1  | 1  | 0  | LS1    | read/write | LED4 to LED7 selector |

## 6.3 Register descriptions

### 6.3.1 INPUT - Input register

The INPUT register reflects the state of the device pins. Writes to this register will be acknowledged but will have no effect.

Table 4. INPUT - Input register description

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | LED7 | LED6 | LED5 | LED4 | LED3 | LED2 | LED1 | LED0 |
| Default | X    | X    | X    | X    | X    | X    | X    | X    |

**Remark:** The default value 'X' is determined by the externally applied logic level (normally logic 1) when used for directly driving LED with pull-up to V<sub>DD</sub>.

**6.3.2 PCS0 - Frequency Prescaler 0**

PSC0 is used to program the period of the PWM output.

The period of BLINK0 = (PSC0 + 1) / 152.

**Table 5. PSC0 - Frequency Prescaler 0 register description**

| Bit     | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Symbol  | PSC0[7] | PSC0[6] | PSC0[5] | PSC0[4] | PSC0[3] | PSC0[2] | PSC0[1] | PSC0[0] |
| Default | 1       | 1       | 1       | 1       | 1       | 1       | 1       | 1       |

**6.3.3 PWM0 - Pulse Width Modulation 0**

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED on) when the count is less than the value in PWM0 and HIGH (LED off) when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always HIGH (LED off).

The duty cycle of BLINK0 = PWM0 / 256.

**Table 6. PWM0 - Pulse Width Modulation 0 register description**

| Bit     | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Symbol  | PWM0 [7] | PWM0 [6] | PWM0 [5] | PWM0 [4] | PWM0 [3] | PWM0 [2] | PWM0 [1] | PWM0 [0] |
| Default | 1        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

**6.3.4 PCS1 - Frequency Prescaler 1**

PSC1 is used to program the period of the PWM output.

The period of BLINK1 = (PSC1 + 1) / 152.

**Table 7. PSC1 - Frequency Prescaler 1 register description**

| Bit     | 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Symbol  | PSC1[7] | PSC1[6] | PSC1[5] | PSC1[4] | PSC1[3] | PSC1[2] | PSC1[1] | PSC1[0] |
| Default | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       |

**6.3.5 PWM1 - Pulse Width Modulation 1**

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED on) when the count is less than the value in PWM1 and HIGH (LED off) when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always HIGH (LED off).

The duty cycle of BLINK1 = PWM1 / 256.

**Table 8. PWM1 - Pulse Width Modulation 1 register description**

| Bit     | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Symbol  | PWM1 [7] | PWM1 [6] | PWM1 [5] | PWM1 [4] | PWM1 [3] | PWM1 [2] | PWM1 [1] | PWM1 [0] |
| Default | 1        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

**6.3.6 LS0 to LS1 - LED selector registers**

The LSn LED select registers determine the source of the LED data.

- 00 = output is set high-impedance (LED off; default)
- 01 = output is set LOW (LED on)
- 10 = output blinks at PWM0 rate
- 11 = output blinks at PWM1 rate

**Table 9. LS0 to LS1 - LED selector registers bit description**

Legend: \* default value.

| Register                           | Bit | Value | Description   |
|------------------------------------|-----|-------|---------------|
| <b>LS0 - LED0 to LED3 selector</b> |     |       |               |
| LS0                                | 7:6 | 00*   | LED3 selected |
|                                    | 5:4 | 00*   | LED2 selected |
|                                    | 3:2 | 00*   | LED1 selected |
|                                    | 1:0 | 00*   | LED0 selected |
| <b>LS1 - LED4 to LED7 selector</b> |     |       |               |
| LS1                                | 7:6 | 00*   | LED7 selected |
|                                    | 5:4 | 00*   | LED6 selected |
|                                    | 3:2 | 00*   | LED5 selected |
|                                    | 1:0 | 00*   | LED4 selected |

**6.4 Pins used as GPIOs**

LED pins not used to control LEDs can be used as General Purpose I/Os (GPIOs).

For use as input, set LEDn to high-impedance (00) and then read the pin state via the Input register.

For use as output, connect external pull-up resistor to the pin and size it according to the DC recommended operating characteristics. LEDn output pin is HIGH when the output is programmed as high-impedance, and LOW when the output is programmed LOW through the 'LED selector' register. The output can be pulse-width controlled when PWM0 or PWM1 are used.

**6.5 Power-on reset**

When power is applied to V<sub>DD</sub>, an internal Power-On Reset (POR) holds the PCA9531 in a reset condition until V<sub>DD</sub> has reached V<sub>POR</sub>. At that point, the reset condition is released and the PCA9531 registers are initialized to their default states, all the outputs in the OFF state. Thereafter, V<sub>DD</sub> must be lowered below 0.2 V to reset the device.

**6.6 External RESET**

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin LOW for a minimum of t<sub>w(rst)</sub>. The PCA9531 registers and I<sup>2</sup>C-bus state machine will be held in their default states until the  $\overline{\text{RESET}}$  input is once again HIGH.

This input requires a pull-up resistor to V<sub>DD</sub> if no active connection is used.



## 7. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 8](#)).

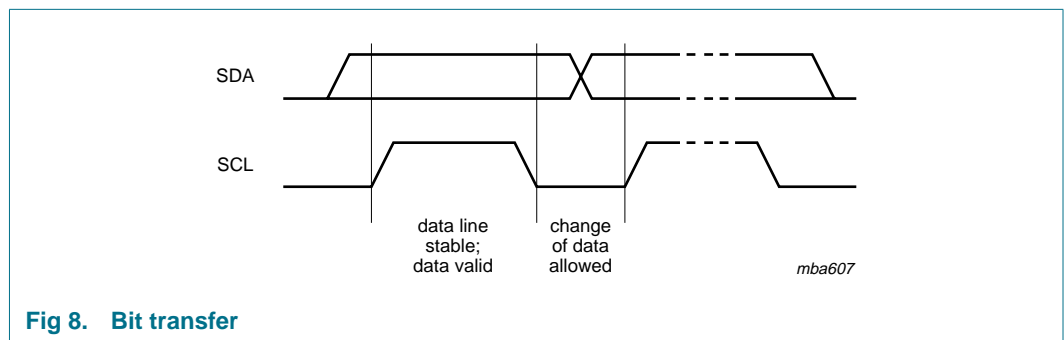


Fig 8. Bit transfer

#### 7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 9](#).)

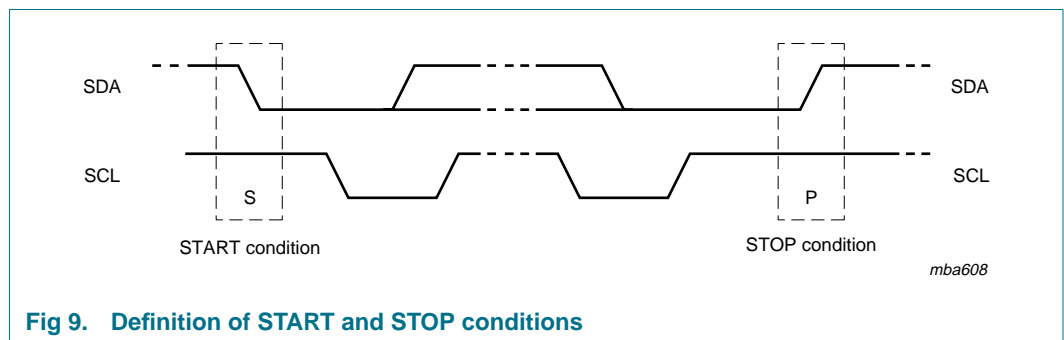


Fig 9. Definition of START and STOP conditions

### 7.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 10](#)).

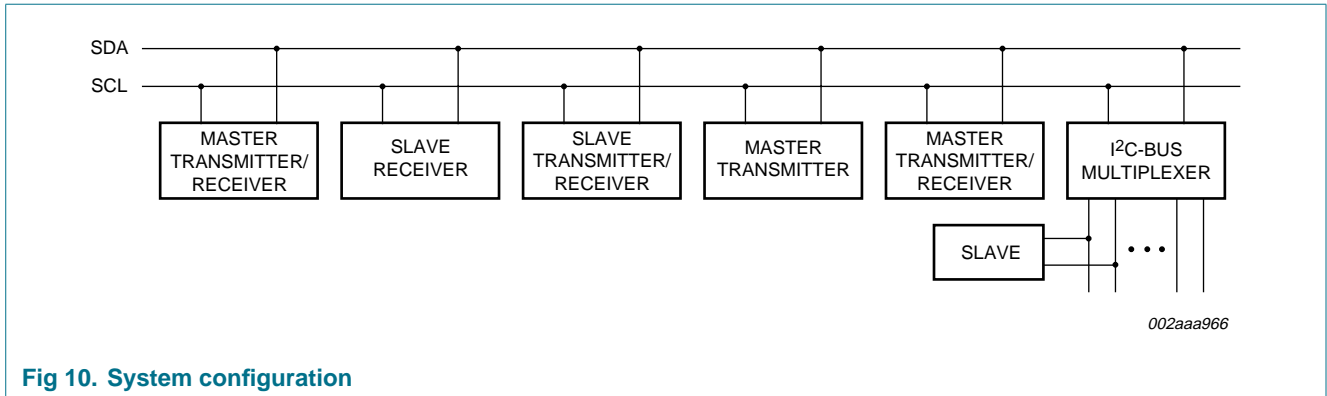


Fig 10. System configuration

### 7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

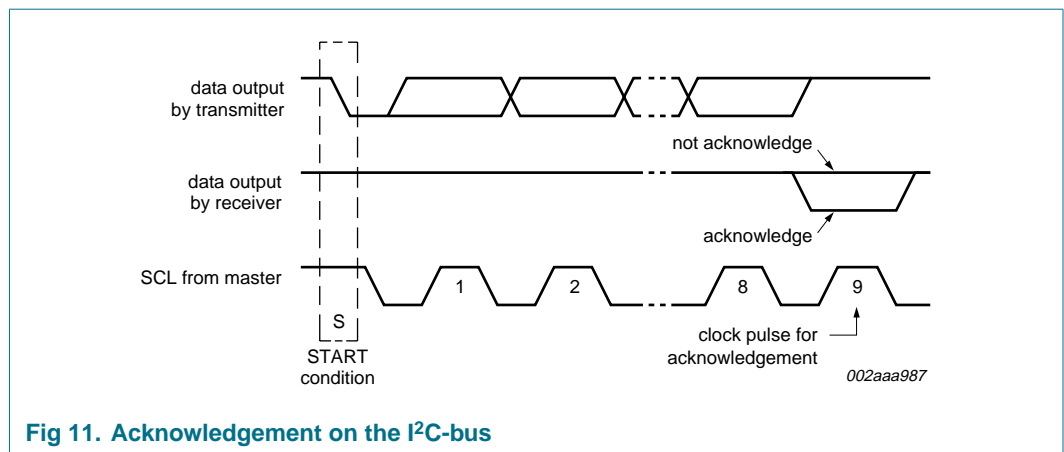
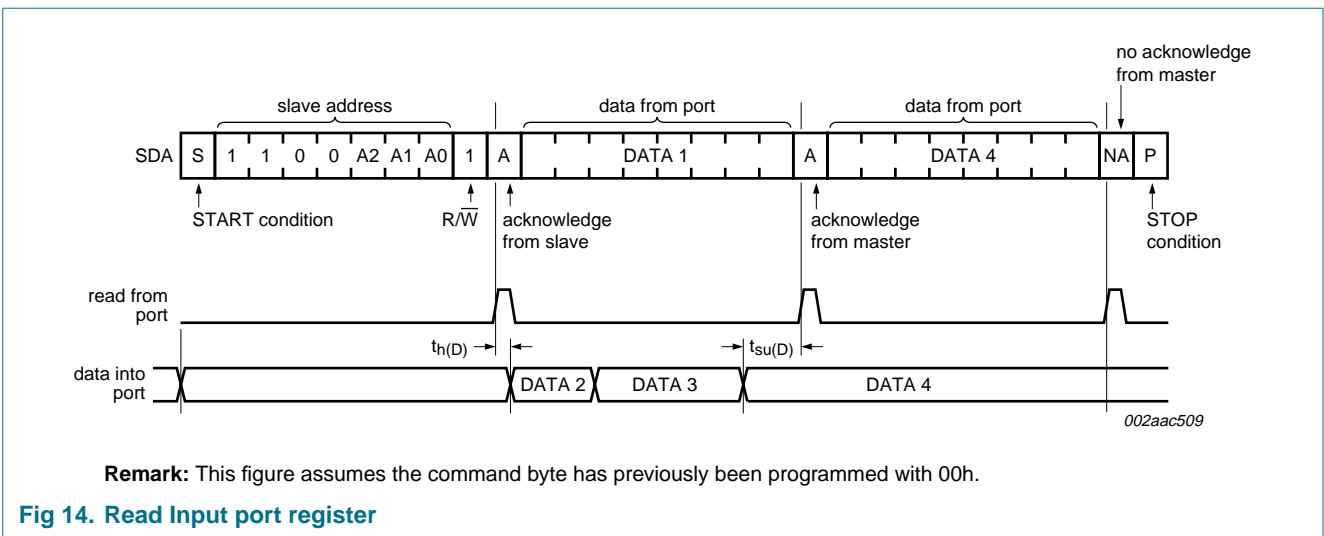
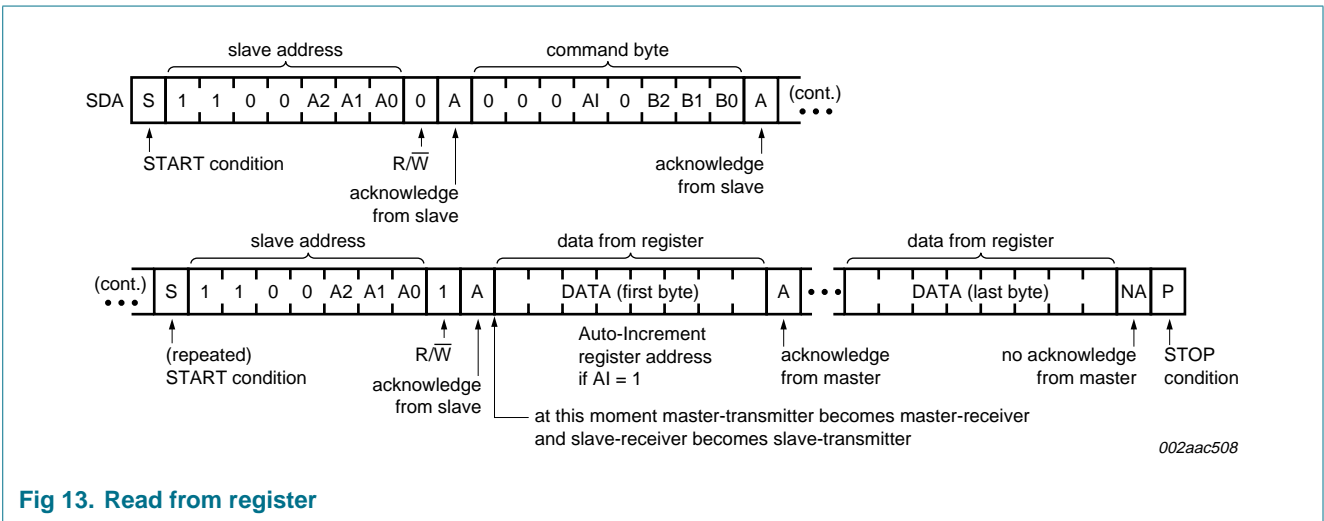
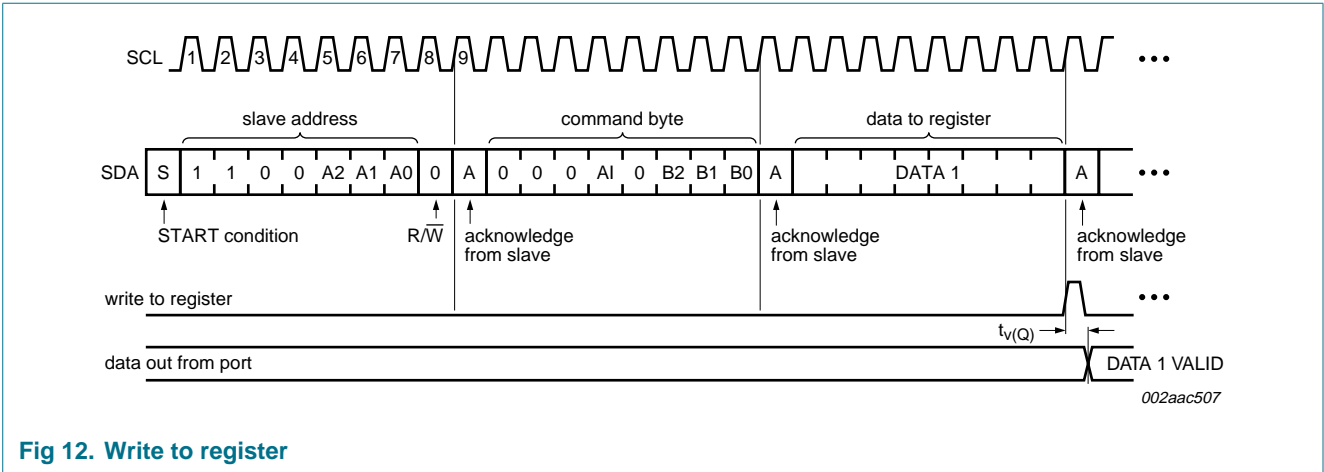
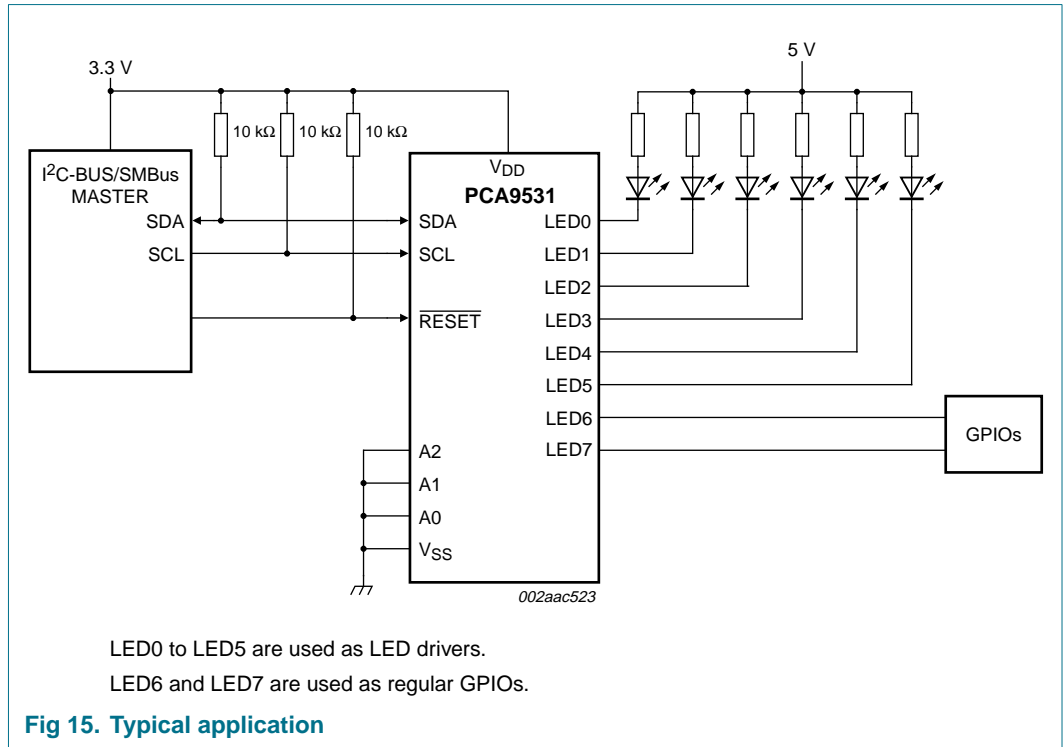


Fig 11. Acknowledgement on the I<sup>2</sup>C-bus

7.4 Bus transactions



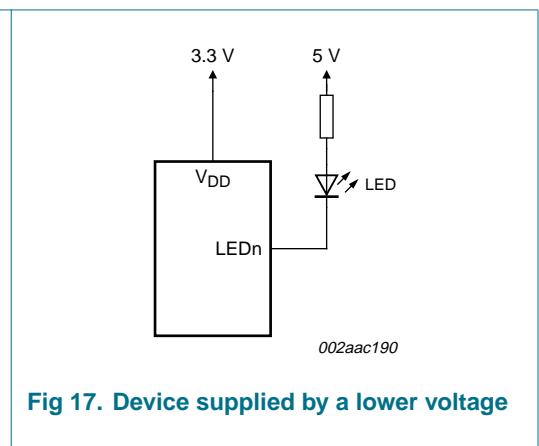
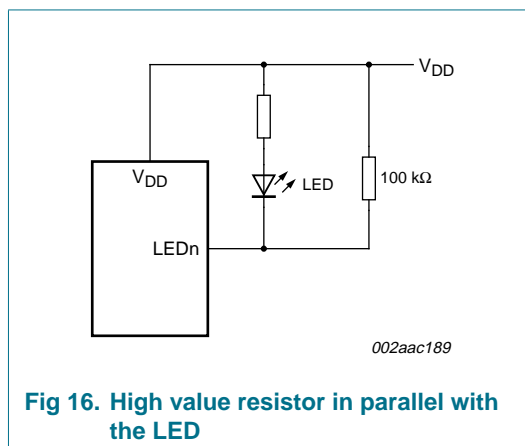
## 8. Application design-in information



### 8.1 Minimizing I<sub>DD</sub> when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V<sub>DD</sub> through a resistor as shown in [Figure 15](#). Since the LED acts as a diode, when the LED is off the I/O V<sub>I</sub> is about 1.2 V less than V<sub>DD</sub>. The supply current, I<sub>DD</sub>, increases as V<sub>I</sub> becomes lower than V<sub>DD</sub> and is specified as ΔI<sub>DD</sub> in [Table 12 “Static characteristics”](#).

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V<sub>DD</sub> when the LED is off. [Figure 16](#) shows a high value resistor in parallel with the LED. [Figure 17](#) shows V<sub>DD</sub> less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V<sub>I</sub> at or above V<sub>DD</sub> and prevents additional supply current consumption when the LED is off.



## 8.2 Programming example

The following example will show how to set LED0 to LED3 on. It will then set LED4 and LED5 to blink at 1 Hz at a 50 % duty cycle. LED6 and LED7 will be set to be dimmed at 25 % of their maximum brightness (duty cycle = 25 %).

**Table 10. Programming PCA9531**

| Program sequence   | I <sup>2</sup> C-bus |
|--|----------------------|
| START  | S                    |
| PCA9531 address with A0 to A2 = LOW  | C0h                  |
| PSC0 subaddress + Auto-Increment   | 11h                  |
| Set prescaler PSC0 to achieve a period of 1 second:<br>$\text{Blink period} = 1 = \frac{\text{PSC0} + 1}{152}$ | 97h                  |
| PSC0 = 151   |                      |
| Set PWM0 duty cycle to 50 %:<br>$\frac{\text{PWM0}}{256} = 0.5$  | 80h                  |
| PWM0 = 128   |                      |
| Set prescaler PCS1 to dim at maximum frequency:<br>$\text{Blink period} = \text{max}$                          | 00h                  |
| PSC1 = 0   |                      |
| Set PWM1 output duty cycle to 25 %:<br>$\frac{\text{PWM1}}{256} = 0.25$  | 40h                  |
| PWM1 = 64  |                      |
| Set LED0 to LED3 on  | 55h                  |
| Set LED4 and LED5 to PWM0, and LED6 or LED7 to PWM1  | FAh                  |
| STOP   | P                    |

## 9. Limiting values

**Table 11. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol               | Parameter                      | Conditions | Min                   | Max  | Unit |
|----------------------|--------------------------------|------------|-----------------------|------|------|
| V <sub>DD</sub>      | supply voltage                 |            | -0.5                  | +6.0 | V    |
| V <sub>I/O</sub>     | voltage on an input/output pin |            | V <sub>SS</sub> - 0.5 | 5.5  | V    |
| I <sub>O(LEDn)</sub> | output current on pin LEDn     |            | -                     | ±25  | mA   |
| I <sub>SS</sub>      | ground supply current          |            | -                     | 200  | mA   |
| P <sub>tot</sub>     | total power dissipation        |            | -                     | 400  | mW   |
| T <sub>stg</sub>     | storage temperature            |            | -65                   | +150 | °C   |
| T <sub>amb</sub>     | ambient temperature            | operating  | -40                   | +85  | °C   |

## 10. Static characteristics

**Table 12. Static characteristics**

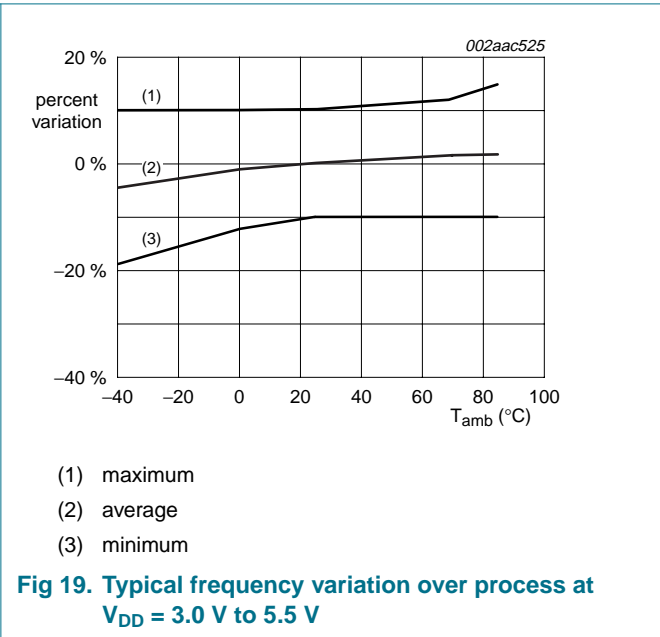
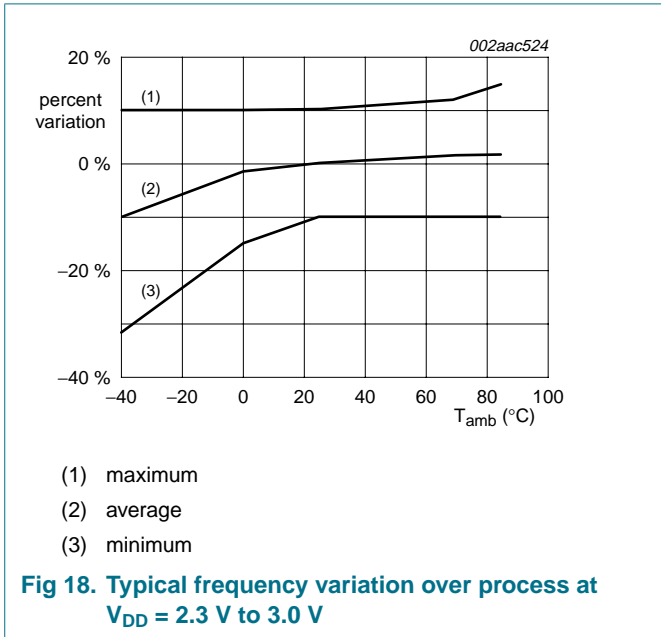
$V_{DD} = 2.3\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

| Symbol                                 | Parameter                           | Conditions   | Min               | Typ <sup>[1]</sup> | Max            | Unit          |
|--|-------------------------------------|--|-------------------|--------------------|----------------|---------------|
| <b>Supplies</b>                        |                                     |  |                   |                    |                |               |
| $V_{DD}$                               | supply voltage                      |  | 2.3               | -                  | 5.5            | V             |
| $I_{DD}$                               | supply current                      | operating mode; $V_{DD} = 5.5\text{ V}$ ;<br>$V_I = V_{DD}$ or $V_{SS}$ ; $f_{SCL} = 100\text{ kHz}$           | -                 | 350                | 500            | $\mu\text{A}$ |
| $I_{stb}$                              | standby current                     | Standby mode; $V_{DD} = 5.5\text{ V}$ ;<br>$V_I = V_{DD}$ or $V_{SS}$ ; $f_{SCL} = 0\text{ kHz}$               | -                 | 1.9                | 3.0            | $\mu\text{A}$ |
| $\Delta I_{DD}$                        | additional quiescent supply current | Standby mode; $V_{DD} = 5.5\text{ V}$ ;<br>every LED I/O at $V_I = 4.3\text{ V}$ ;<br>$f_{SCL} = 0\text{ kHz}$ | -                 | -                  | 800            | $\mu\text{A}$ |
| $V_{POR}$                              | power-on reset voltage              | no load; $V_I = V_{DD}$ or $V_{SS}$  | <sup>[2]</sup> -  | 1.7                | 2.2            | V             |
| <b>Input SCL; input/output SDA</b>     |                                     |  |                   |                    |                |               |
| $V_{IL}$                               | LOW-level input voltage             |  | -0.5              | -                  | +0.3 $V_{DD}$  | V             |
| $V_{IH}$                               | HIGH-level input voltage            |  | 0.7 $V_{DD}$      | -                  | 5.5            | V             |
| $I_{OL}$                               | LOW-level output current            | $V_{OL} = 0.4\text{ V}$  | 3                 | 6.5                | -              | mA            |
| $I_L$                                  | leakage current                     | $V_I = V_{DD} = V_{SS}$  | -1                | -                  | +1             | $\mu\text{A}$ |
| $C_i$                                  | input capacitance                   | $V_I = V_{SS}$   | -                 | 3.7                | 5              | pF            |
| <b>I/Os</b>                            |                                     |  |                   |                    |                |               |
| $V_{IL}$                               | LOW-level input voltage             |  | -0.5              | -                  | +0.8           | V             |
| $V_{IH}$                               | HIGH-level input voltage            |  | 2.0               | -                  | 5.5            | V             |
| $I_{OL}$                               | LOW-level output current            | $V_{OL} = 0.4\text{ V}$  |                   |                    |                |               |
|  |                                     | $V_{DD} = 2.3\text{ V}$  | <sup>[3]</sup> 9  | -                  | -              | mA            |
|  |                                     | $V_{DD} = 3.0\text{ V}$  | <sup>[3]</sup> 12 | -                  | -              | mA            |
|  |                                     | $V_{DD} = 5.0\text{ V}$  | <sup>[3]</sup> 15 | -                  | -              | mA            |
|  |                                     | $V_{OL} = 0.7\text{ V}$  |                   |                    |                |               |
|  |                                     | $V_{DD} = 2.3\text{ V}$  | <sup>[3]</sup> 15 | -                  | -              | mA            |
|  |                                     | $V_{DD} = 3.0\text{ V}$  | <sup>[3]</sup> 20 | -                  | -              | mA            |
|  |                                     | $V_{DD} = 5.0\text{ V}$  | <sup>[3]</sup> 25 | -                  | -              | mA            |
| $I_L$                                  | input leakage current               | $V_{DD} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$ or $V_{DD}$   | -1                | -                  | +1             | $\mu\text{A}$ |
| $C_{io}$                               | input/output capacitance            |  | -                 | 2.5                | 5              | pF            |
| <b>Select inputs A0, A1, A2; RESET</b> |                                     |  |                   |                    |                |               |
| $V_{IL}$                               | LOW-level input voltage             |  | -0.5              | -                  | +0.8           | V             |
| $V_{IH}$                               | HIGH-level input voltage            | A0; $\overline{\text{RESET}}$  | 2.0               | -                  | 5.5            | V             |
|  |                                     | A1; A2   | 2.0               | -                  | $V_{DD} + 0.5$ | V             |
| $I_{LI}$                               | input leakage current               |  | -1                | -                  | +1             | $\mu\text{A}$ |
| $C_i$                                  | input capacitance                   | $V_I = V_{SS}$   | -                 | 2.3                | 5              | pF            |

[1] Typical limits at  $V_{DD} = 3.3\text{ V}$ ,  $T_{amb} = 25\text{ °C}$ .

[2]  $V_{DD}$  must be lowered to 0.2 V in order to reset part.

[3] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.



## 11. Dynamic characteristics

Table 13. Dynamic characteristics

| Symbol                | Parameter   | Conditions | Standard-mode I <sup>2</sup> C-bus |      | Fast-mode I <sup>2</sup> C-bus |     | Unit |
|-----------------------|---|------------|------------------------------------|------|--------------------------------|-----|------|
|                       |   |            | Min                                | Max  | Min                            | Max |      |
| f <sub>SCL</sub>      | SCL clock frequency   |            | 0                                  | 100  | 0                              | 400 | kHz  |
| t <sub>BUF</sub>      | bus free time between a STOP and START condition                  |            | 4.7                                | -    | 1.3                            | -   | μs   |
| t <sub>HD,STA</sub>   | hold time (repeated) START condition                              |            | 4.0                                | -    | 0.6                            | -   | μs   |
| t <sub>SU,STA</sub>   | set-up time for a repeated START condition                        |            | 4.7                                | -    | 0.6                            | -   | μs   |
| t <sub>SU,STO</sub>   | set-up time for STOP condition                                    |            | 4.0                                | -    | 0.6                            | -   | μs   |
| t <sub>HD,DAT</sub>   | data hold time  |            | 0                                  | -    | 0                              | -   | ns   |
| t <sub>VD,ACK</sub>   | data valid acknowledge time                                       |            | [1]                                | 600  | -                              | 600 | ns   |
| t <sub>VD,DAT</sub>   | data valid time   | LOW-level  | [2]                                | 600  | -                              | 600 | ns   |
|                       |   | HIGH-level | [2]                                | 1500 | -                              | 600 | ns   |
| t <sub>SU,DAT</sub>   | data set-up time  |            | 250                                | -    | 100                            | -   | ns   |
| t <sub>LOW</sub>      | LOW period of the SCL clock                                       |            | 4.7                                | -    | 1.3                            | -   | μs   |
| t <sub>HIGH</sub>     | HIGH period of the SCL clock                                      |            | 4.0                                | -    | 0.6                            | -   | μs   |
| t <sub>r</sub>        | rise time of both SDA and SCL signals                             |            | -                                  | 1000 | 20 + 0.1C <sub>b</sub> [3]     | 300 | ns   |
| t <sub>f</sub>        | fall time of both SDA and SCL signals                             |            | -                                  | 300  | 20 + 0.1C <sub>b</sub> [3]     | 300 | ns   |
| t <sub>SP</sub>       | pulse width of spikes that must be suppressed by the input filter |            | -                                  | 50   | -                              | 50  | ns   |
| <b>Port timing</b>    |   |            |                                    |      |                                |     |      |
| t <sub>V(Q)</sub>     | data output valid time  |            | -                                  | 200  | -                              | 200 | ns   |
| t <sub>SU(D)</sub>    | data input setup time   |            | 100                                | -    | 100                            | -   | ns   |
| t <sub>H(D)</sub>     | data input hold time  |            | 1                                  | -    | 1                              | -   | μs   |
| <b>Reset</b>          |   |            |                                    |      |                                |     |      |
| t <sub>w(rst)</sub>   | reset pulse width   |            | 6                                  | -    | 6                              | -   | ns   |
| t <sub>rec(rst)</sub> | reset recovery time   |            | 0                                  | -    | 0                              | -   | ns   |
| t <sub>rst</sub>      | reset time  | [4][5]     | 400                                | -    | 400                            | -   | ns   |

[1] t<sub>VD,ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] t<sub>VD,DAT</sub> = minimum time for SDA data output to be valid following SCL LOW.

[3] C<sub>b</sub> = total capacitance of one bus line in pF.

[4] Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.

[5] Upon reset, the full delay will be the sum of t<sub>rst</sub> and the RC time constant of the SDA bus.



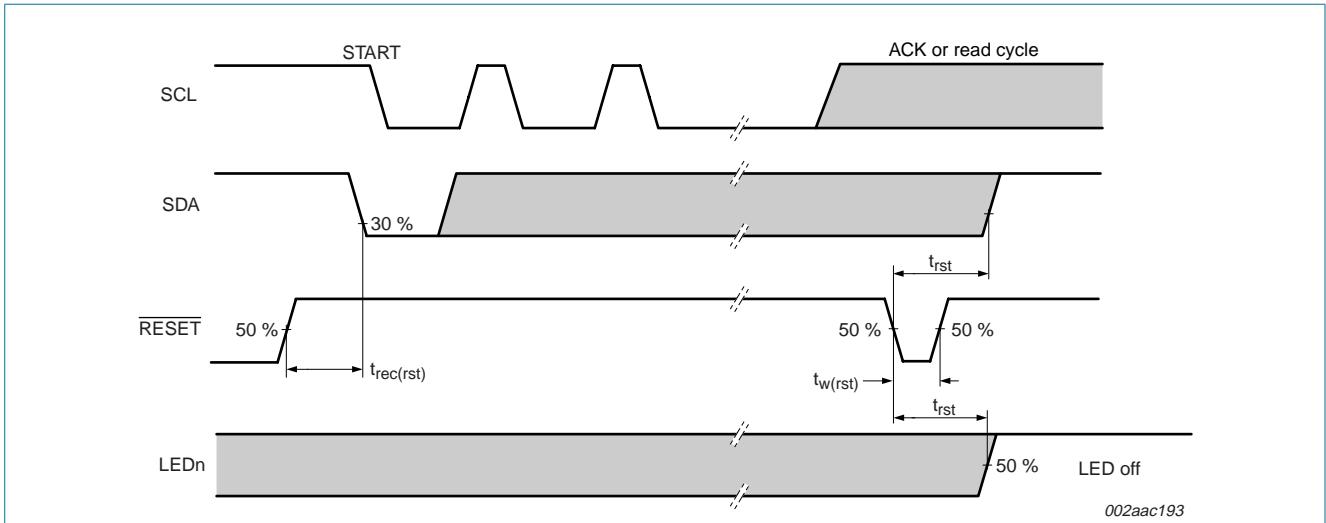


Fig 20. Definition of RESET timing

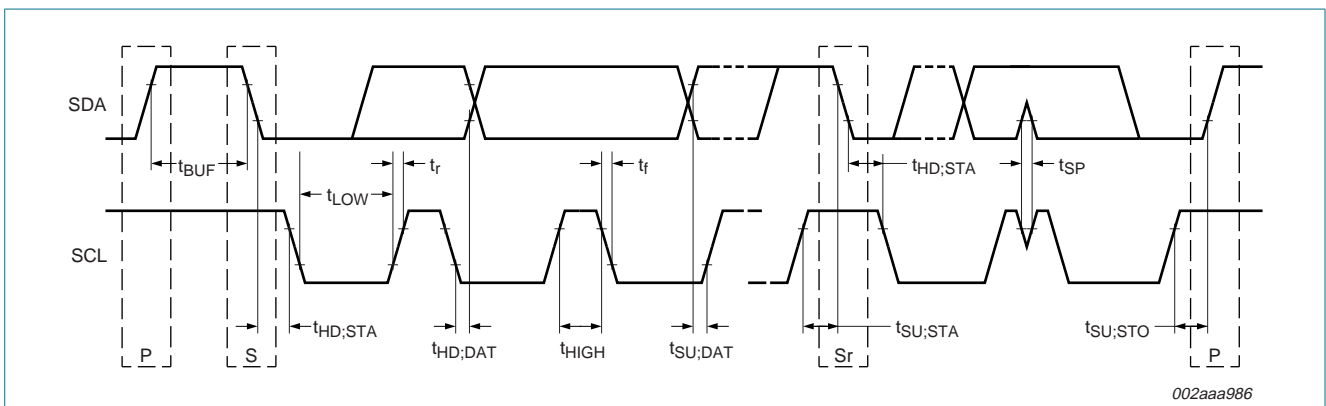
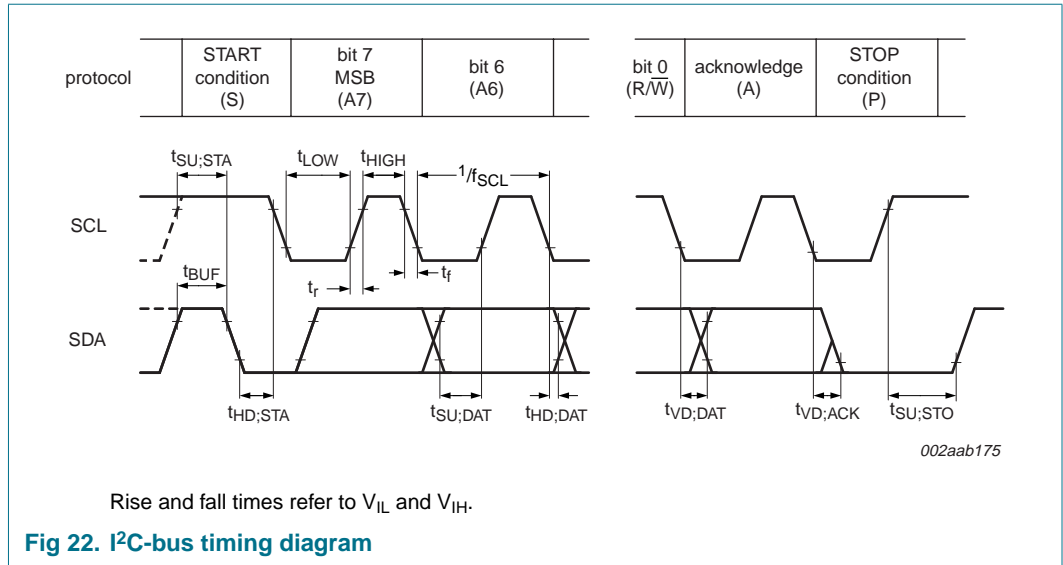
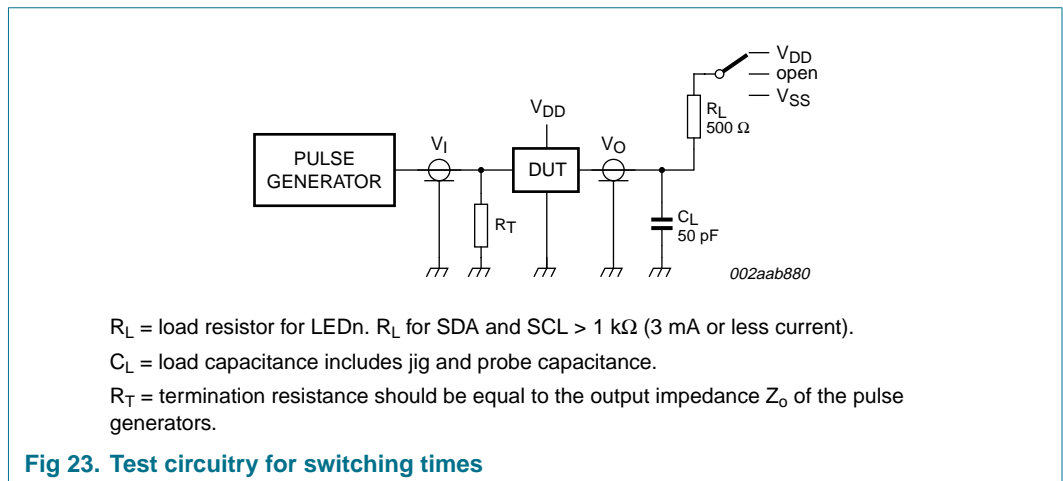


Fig 21. Definition of timing



## 12. Test information



13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

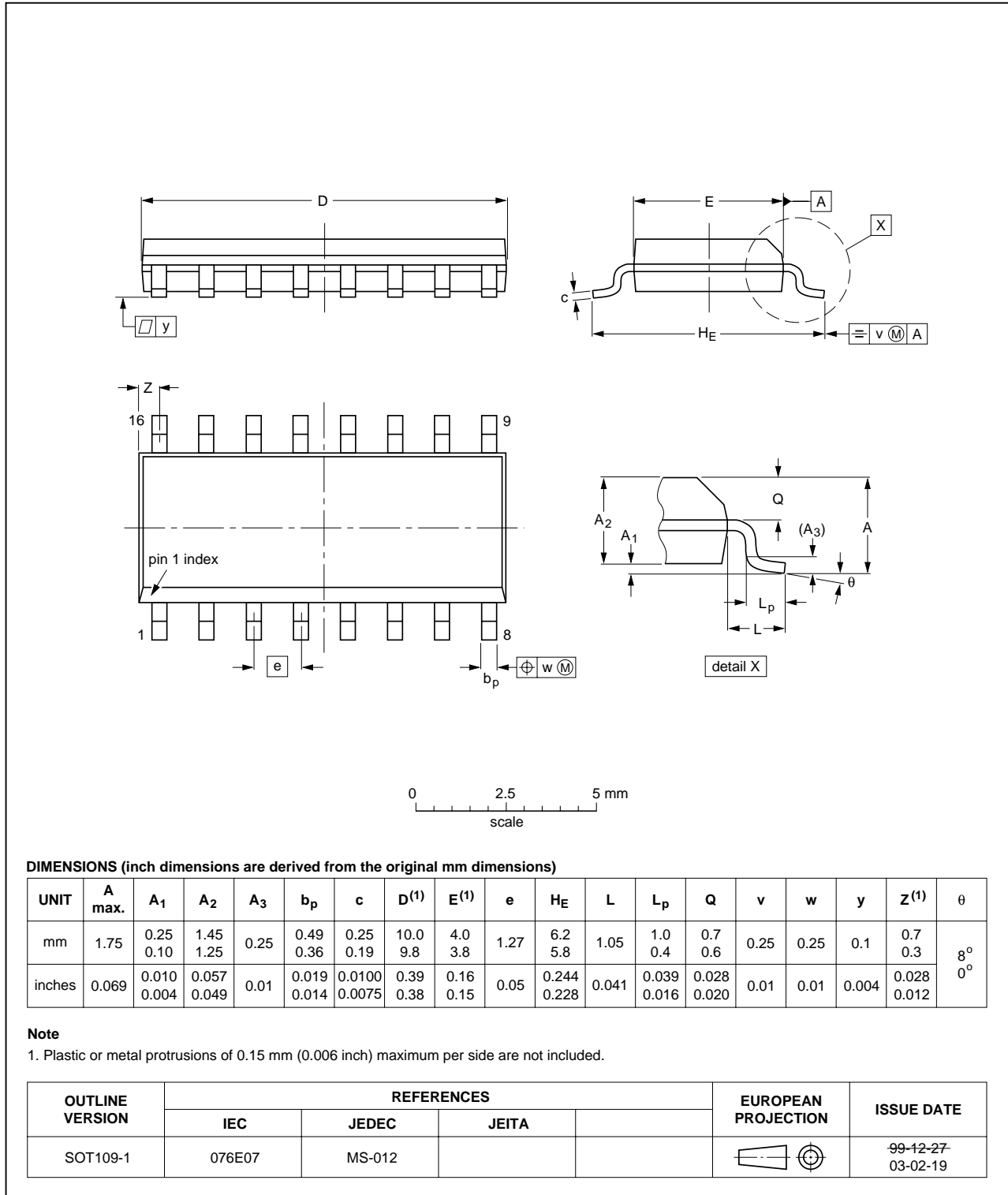


Fig 24. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

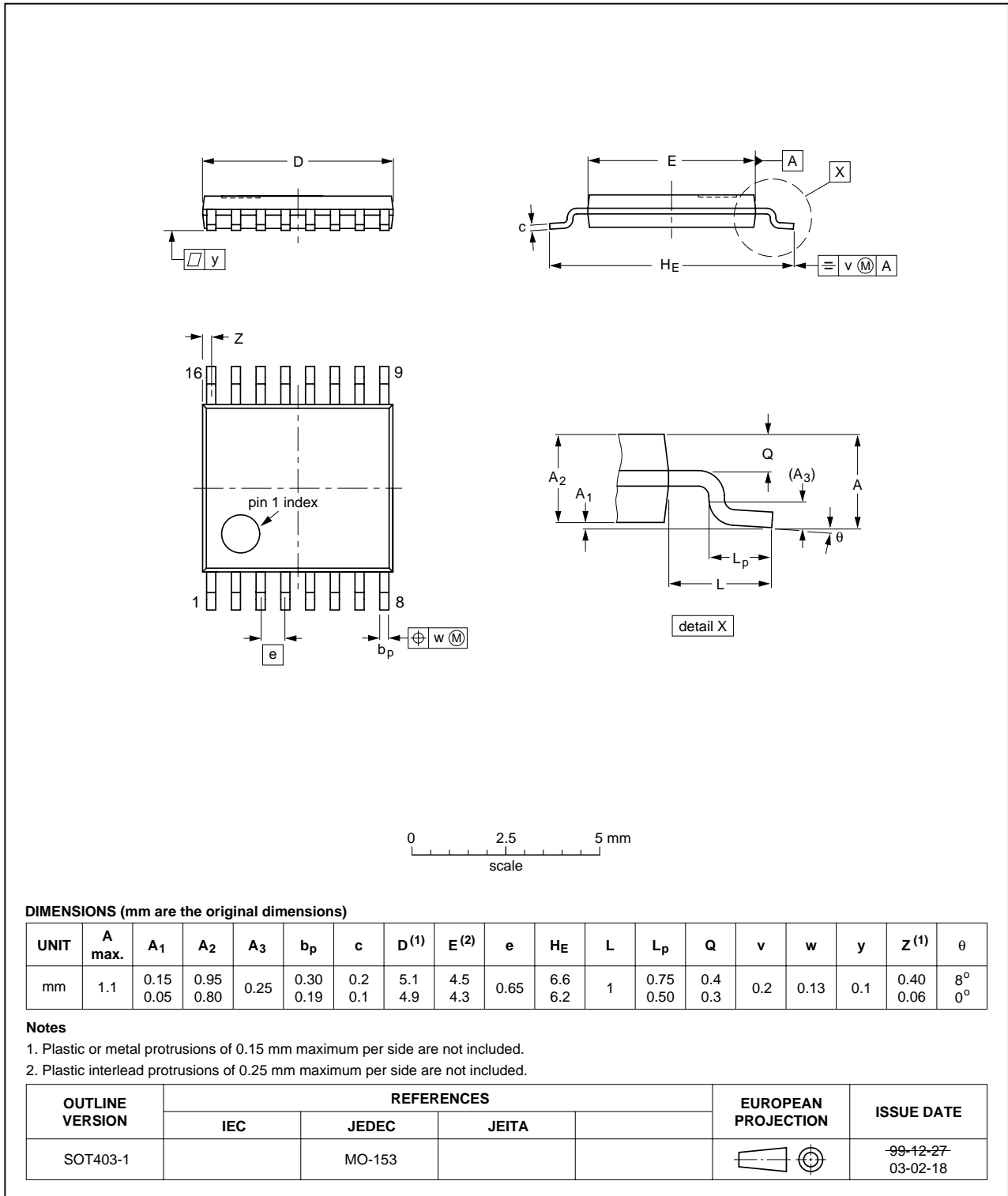
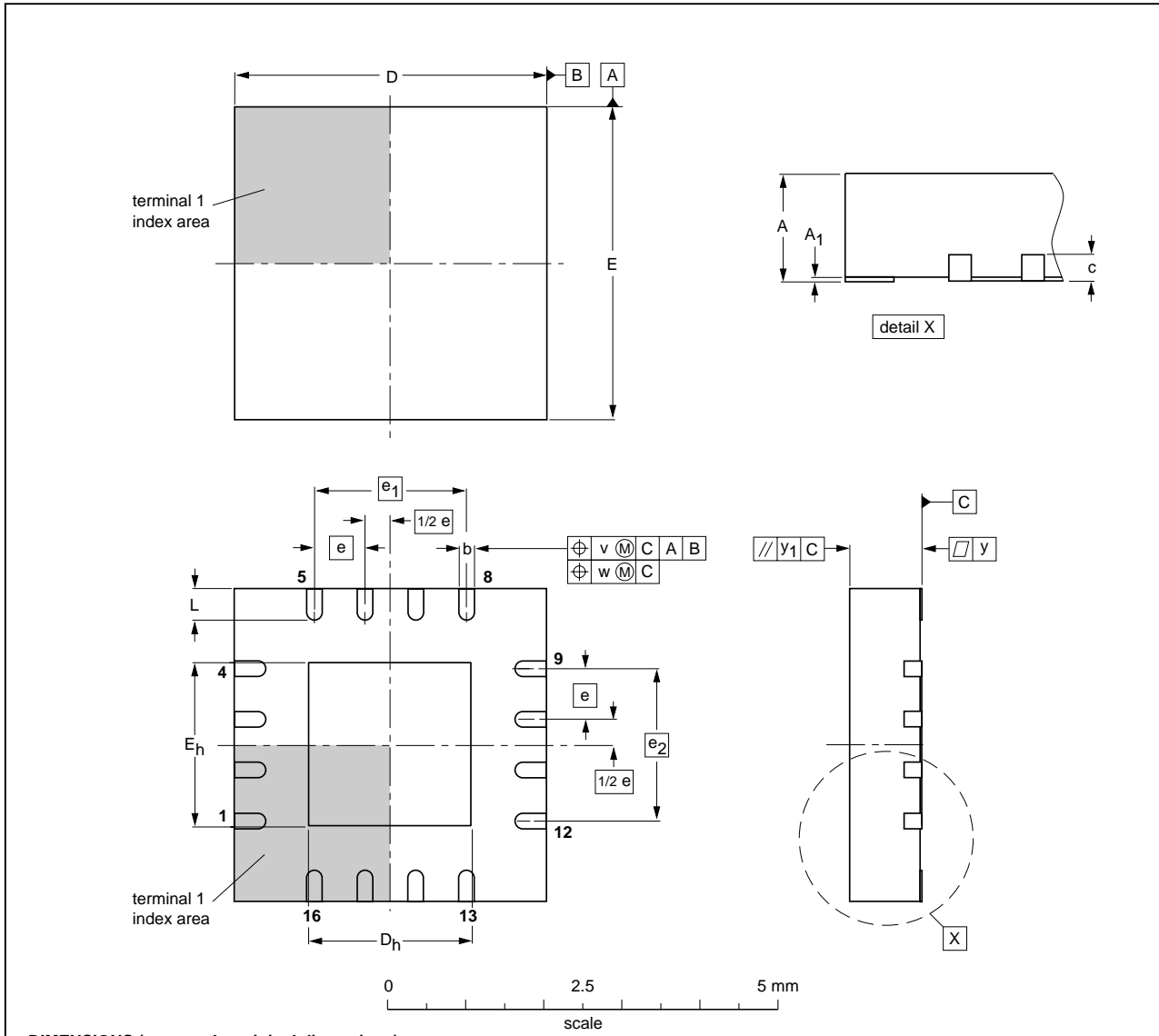


Fig 25. Package outline SOT403-1 (TSSOP16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm

SOT629-1



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A <sup>(1)</sup> max. | A <sub>1</sub> | b            | c   | D <sup>(1)</sup> | D <sub>h</sub> | E <sup>(1)</sup> | E <sub>h</sub> | e    | e <sub>1</sub> | e <sub>2</sub> | L            | v   | w    | y    | y <sub>1</sub> |
|------|-----------------------|----------------|--------------|-----|------------------|----------------|------------------|----------------|------|----------------|----------------|--------------|-----|------|------|----------------|
| mm   | 1                     | 0.05<br>0.00   | 0.38<br>0.23 | 0.2 | 4.1<br>3.9       | 2.25<br>1.95   | 4.1<br>3.9       | 2.25<br>1.95   | 0.65 | 1.95           | 1.95           | 0.75<br>0.50 | 0.1 | 0.05 | 0.05 | 0.1            |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |       |  | EUROPEAN PROJECTION | ISSUE DATE            |
|-----------------|------------|--------|-------|--|---------------------|-----------------------|
|                 | IEC        | JEDEC  | JEITA |  |                     |                       |
| SOT629-1        | ---        | MO-220 | ---   |  |                     | 01-08-08-<br>02-10-22 |

Fig 26. Package outline SOT629-1 (HVQFN16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm

SOT758-1

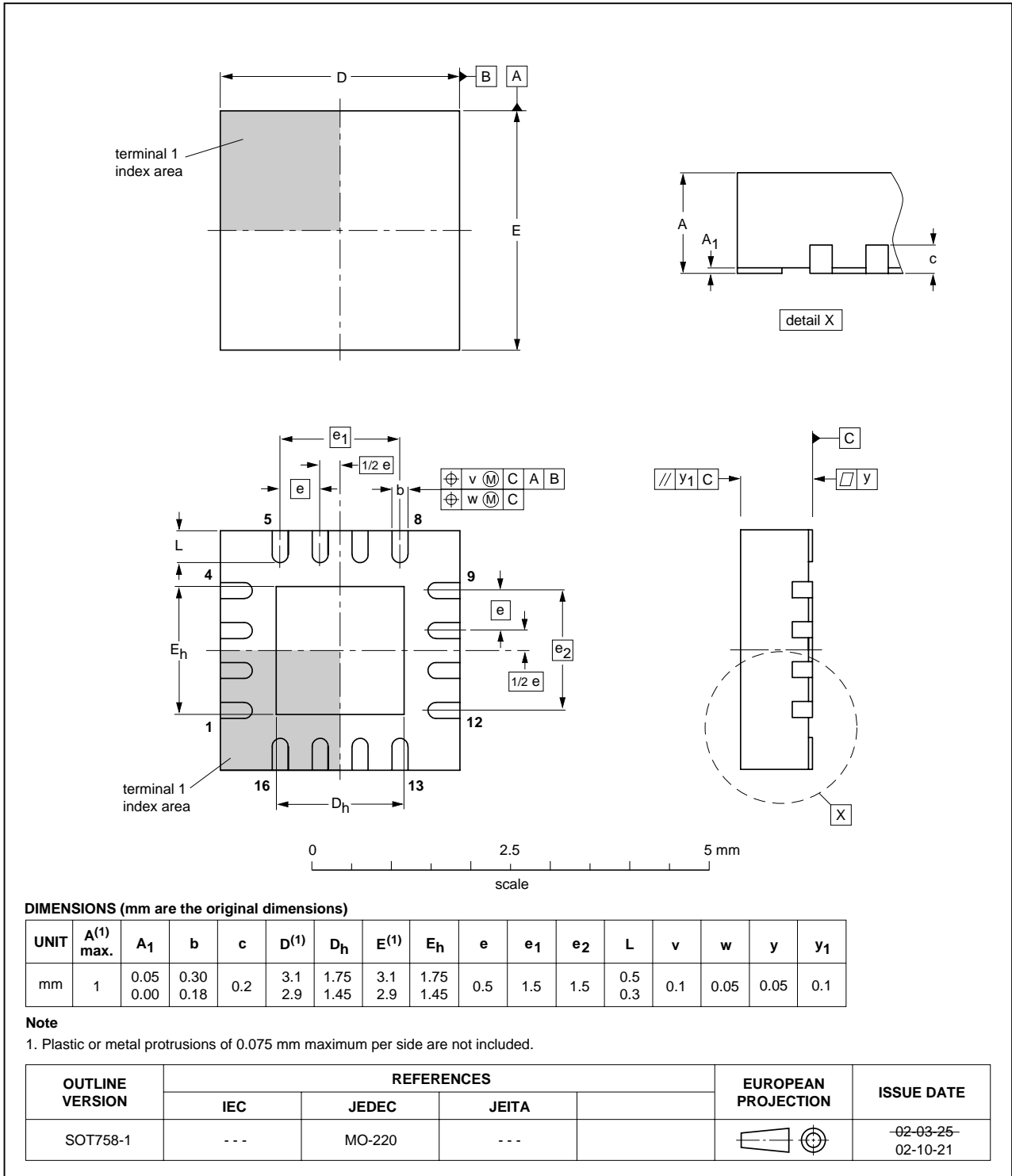


Fig 27. Package outline SOT758-1 (HVQFN16)

## 14. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

## 15. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 28](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 14](#) and [15](#)

**Table 14. SnPb eutectic process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

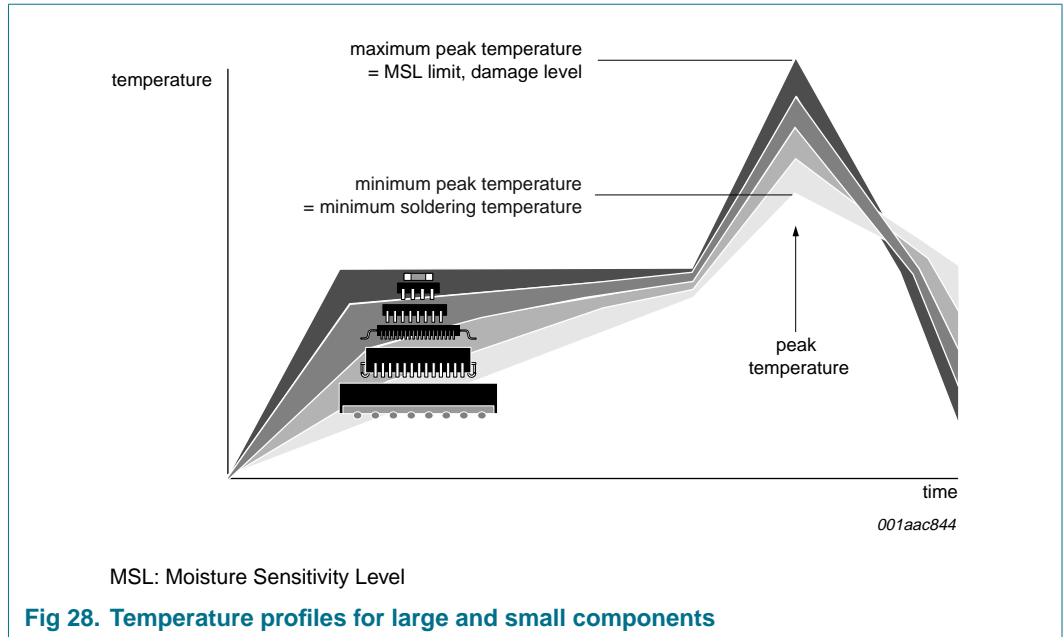
**Table 15. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 28](#).





For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 16. Abbreviations

**Table 16. Abbreviations**

| Acronym              | Description                  |
|----------------------|------------------------------|
| CDM                  | Charged Device Model         |
| DSP                  | Digital Signal Processor     |
| DUT                  | Device Under Test            |
| ESD                  | ElectroStatic Discharge      |
| GPIO                 | General Purpose Input/Output |
| HBM                  | Human Body Model             |
| I <sup>2</sup> C-bus | Inter-Integrated Circuit bus |
| LED                  | Light Emitting Diode         |
| MCU                  | Microcontroller              |
| MM                   | Machine Model                |
| MPU                  | Microprocessor               |
| POR                  | Power-On Reset               |
| RC                   | Resistor-Capacitor network   |
| SMBus                | System Management Bus        |

## 17. Revision history

**Table 17. Revision history**

| Document ID                   | Release date  | Data sheet status  | Change notice                | Supersedes |
|-------------------------------|---|--------------------|------------------------------|------------|
| PCA9531_5                     | 20070912  | Product data sheet | -                            | PCA9531_4  |
| Modifications:                | • Added PCA9531BS3, HVQFN16 (SOT758-1) package offering |                    |                              |            |
| PCA9531_4                     | 20070226  | Product data sheet | -                            | PCA9531_3  |
| PCA9531_3                     | 20061102  | Product data sheet | -                            | PCA9531_2  |
| PCA9531_2<br>(9397 750 13689) | 20041001  | Product data sheet | -                            | PCA9531_1  |
| PCA9531_1<br>(9397 750 12292) | 20031110  | Product data       | 853-2407 30411<br>(20030906) | -          |

## 18. Legal information

### 18.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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